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TFT LCD Engineering Specification

MODEL No.: R208R3-L01

Type 20.8 QXGA Color LCD Module

Approval (Ver 2.1)

IDTech

Customer: _____

Approved by: _____

Note:

記錄	工作	審核	角色	投票
2007-10-26 15:15:32 CST	PMMD Director	Jessiechu (朱砡瑩/12220)	Director	Accept

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REVISION HISTORY

Version	Date	Section	Description
Ver 0.0	Dec.12, '06	All	R208R3 -L01 Specifications was first issued.
	Dec. 08, '06	All	Revised and for customer distribution. Approved by CMO Japan.
Ver 0.1	Dec. 28, '06	5.1	Correction
		5.2	Correction
Ver 0.2	Mar. 20, '07	8.0	New Added, I2C Specification
Ver 0.3	May, 28, '07	5.2	Note (5) description correction,
		6.1	Horizontal Active Display Term Blank spec update :
		8.0	Description correction,
Ver 1.0	June, 28, '07	7.2	New added, Image Retention Specification
		8.2	Correction, the select command of gamma table
Ver2.0	Aug.,20, '07	3.3	New Added, VDIM vs Dimming Range Chart
		10.0	Add IDTech Logo on ID Label
Ver2.1	Oct.16, '07	5.2	New Added, Note(6)

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

R208R3-L01is a 20.8" TFT Liquid Crystal Display module with 14 CCFL Backlight unit and two port 31 pins 2ch-LVDS interface. This module supports 2048 x 1536 QXGA screen and can display 16.7M colors driven by 8bit drivers. The LCD module includes built-in inverter for Backlight.

1.2 FEATURES

- This specification applies to the Type 20.8" Color TFT LCD Module, Model R208R3-L01- This module includes an inverter card for the backlight.
- The screen format is intended to support QXGA 2048(H) x 1536(V) resolution.
- Supported colors are native 16M (8-bits data per R, G, B each).
- All input signals are LVDS (Low Voltage Differential Signaling) interface.
- Designed to increase luminance based on ITQX20J
-The contrast was enhanced to enable gray scale application
-

1.3 APPLICATION

- This module is design for a TFT LCD Monitor style display unit.

1.4 GENERAL SPECIFICATI0N

Item	Specification	Unit	Note
Active Area	423.936 (H) x 317.952 (V) (20.8" diagonal)	mm	(1)
Bezel Opening Area	427.9 (H) x 322 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	2048 x R.G.B. x 1536	pixel	-
Pixel Pitch	0.207 (H) x 0.207 (V)	mm	-
Pixel Arrangement	RGB vertical stripe (at landscape position)	-	-
Display Colors	16.7M (8-bits data per R, G, B each)	color	-
Surface Treatment	Hard coating (3H), Anti-glare (Haze 25)	-	-

1.5 MECHANICAL SPECIFICATION

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	456.2	457.0	457.8	mm	(1)
	Vertical(V)	349.2	350.0	350.8	mm	
	Depth(D)	-	45	45.8	mm	
Weight				2580		-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

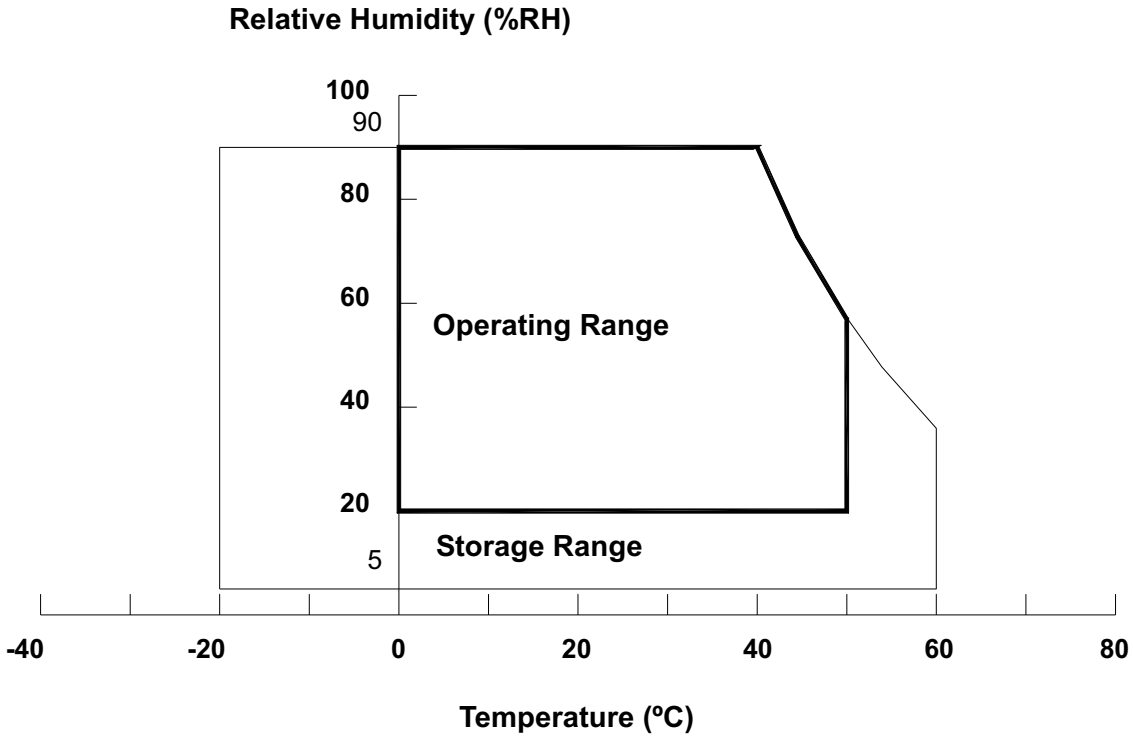
(c) No condensation.

Note (2) The temperature of panel display surface area should be 0 ºC Min. and 60 ºC Max.

Note (3) 11ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 30min/cycle, 1 cycle each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



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2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	+13.2	V	(1)
Logic Input Voltage	V_{logic}	-0.3	4.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	-	2.5K	V_{RMS}	(1), (2), I_L =6mA
Lamp Current	I_L	-	6	mA_{RMS}	
Lamp Frequency	F_L	-	80	KHz	(1), (2)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

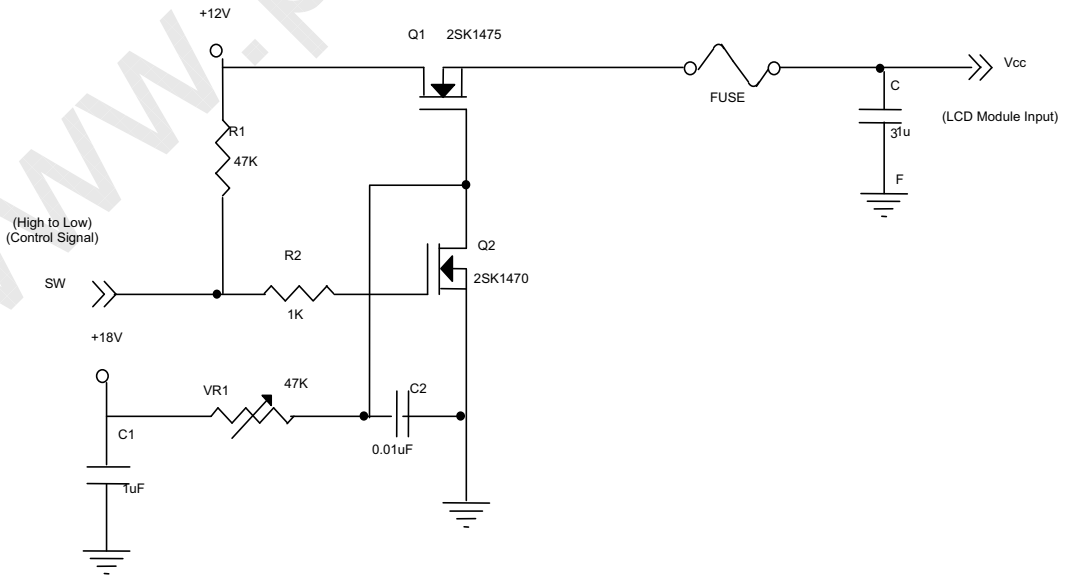
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	11.4	12.0	12.6	V	(1)
Ripple Voltage		V_{RP}	-	-	100	mV	(1)
Rush Current		I_{RUSH}	-	-	3.8	A	(2)
Power Supply Current	White	-		790	1100	mA	(3)a
	Black	-		580	810	mA	(3)b
	Vertical Stripe	-		780	1090	mA	(3)c
LVDS differential input voltage		Vid	100	-	600	mV	
LVDS common input voltage		Vic	-	1.2	-	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



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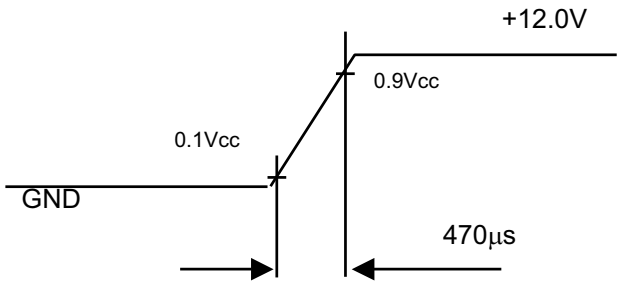
Note (3) The specified power supply current is under the conditions at Vcc = 12.0 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

Vcc rising time is 470μs



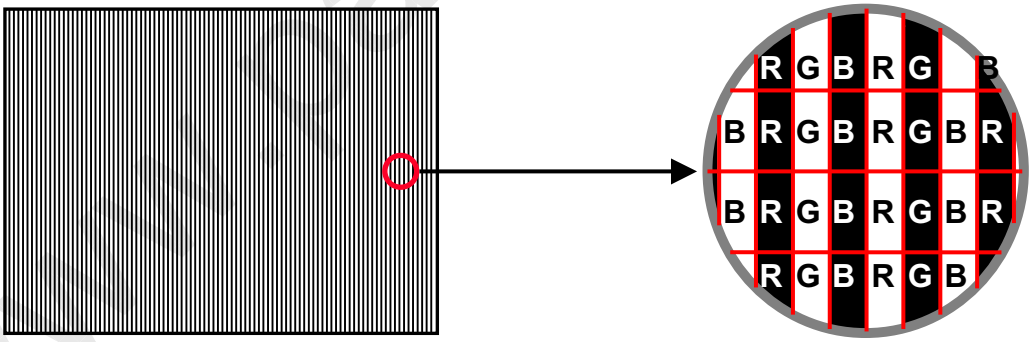
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

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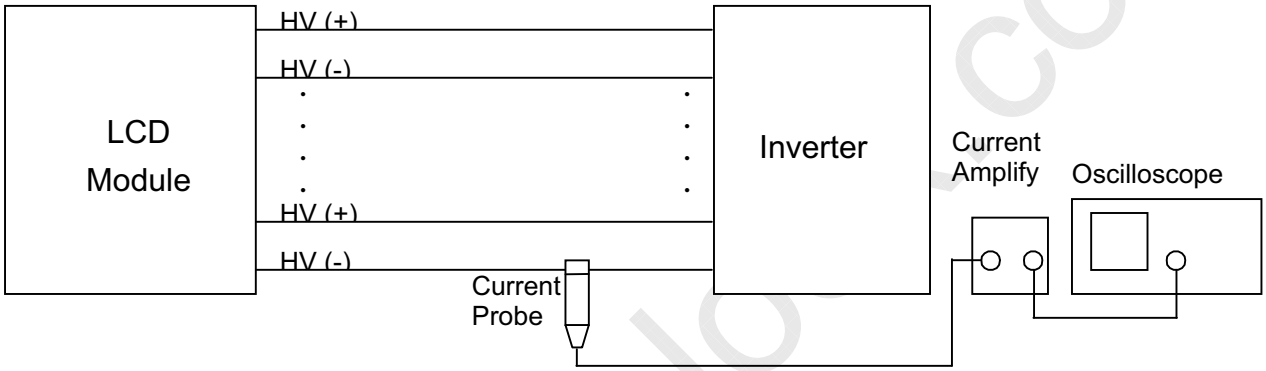
3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	702	780	858	V_{RMS}	(I_L = 6.5 mA)
Lamp Current	I_L	2.0	6.5	7	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	---	---	1540 (25 ºC)	V_{RMS}	(2)
		---	---	1750(0 ºC)	V_{RMS}	(2)
Operating Frequency	F_L	40	---	80	KHz	(3)
Lamp Life Time	L_{BL}	50000 hr	---	---	Hrs	(5)
Power Consumption	P_L	---	70.98	---	W	(4), (I_L = 6.5 mA)

Note (1)Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L \times$ 14 CCFLs

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ±2 °C and I_L = 2.0 ~ 6.5 mArms until one of the following events occurs:

(a) When the brightness becomes or lower than 50% of its original value.

(b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the

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inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

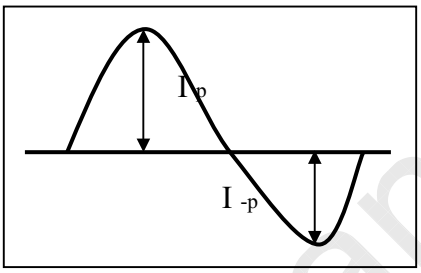
The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter, which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below;

b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;

c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

3.3 Inverter Electrical characteristics

Item	Symbol	Description	Min.	Typ.	Max.	Unit
1	V_{in}	Input voltage	11.2	12	12.8	V
2	I_{in}	Input current (@Vin=12V)	---	6.5	7	A
3	P_{in}	Input power	---	78	84	W
4	BLON	Inverter On/Off control: OFF	-0.1	0	0.8	V
		Inverter On/Off control: ON	2	3.3	6	V
5	VDIM	Output current control VDIM: 0V, maximum brightness VDIM: 3V, minimum brightness	0	---	3	V
6	F_b	Burst Mode Frequency	225	250	275	Hz
7	Freq.	Operating frequency	45	50	55	KHz
8	I_{out}	Output current, VDIM=0V	5.5	6	6.5	mA
9	V_{lamp}	Lamp ignite voltage	1750	---	---	Vrms

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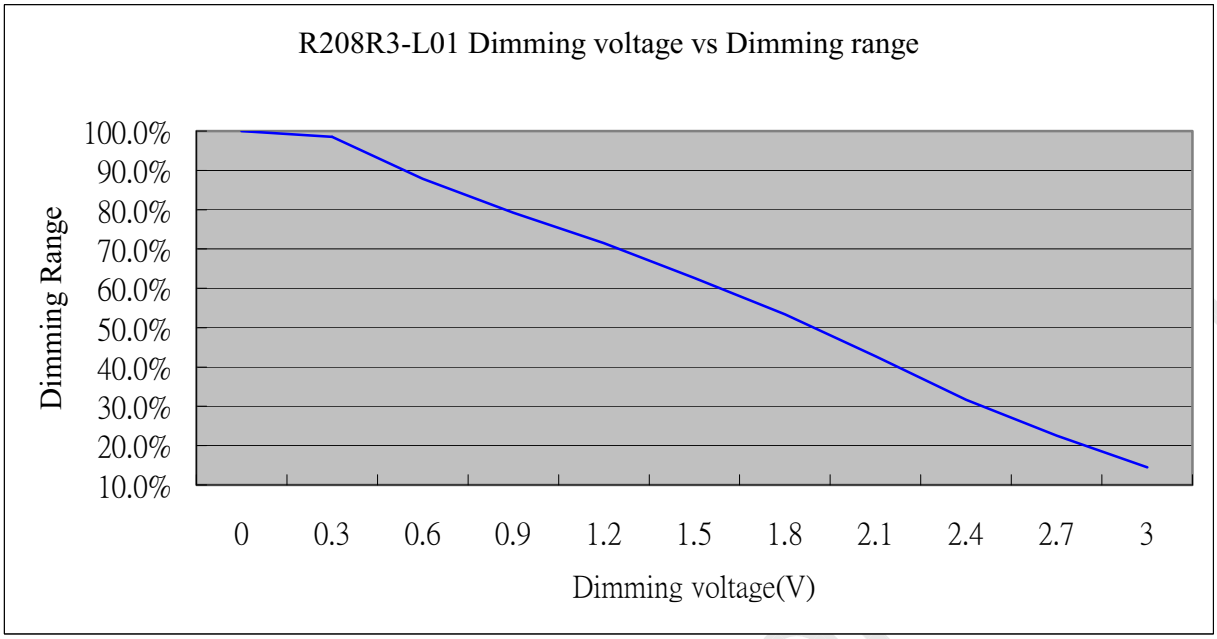
The following chart is the VDIM vs Dimming Range for your reference.



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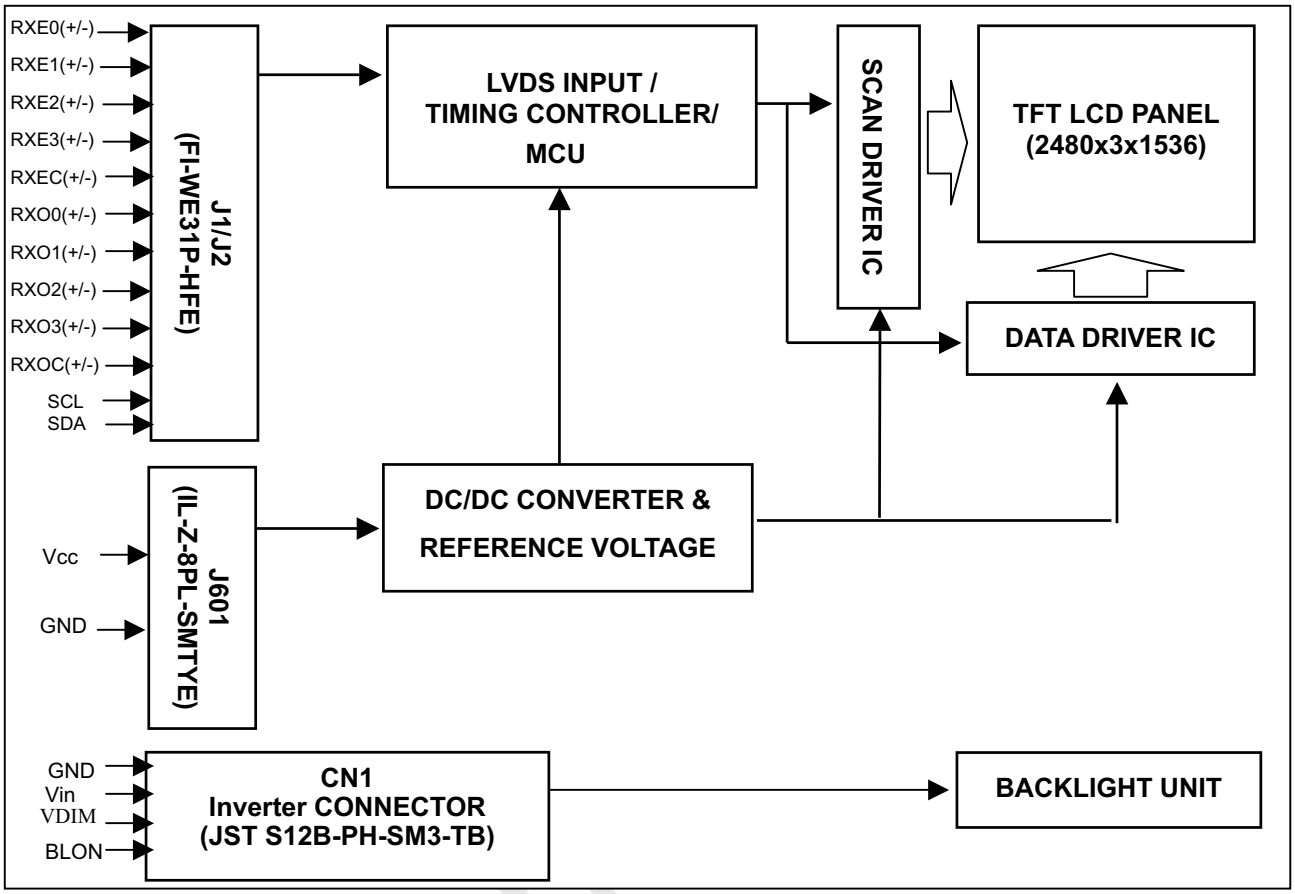
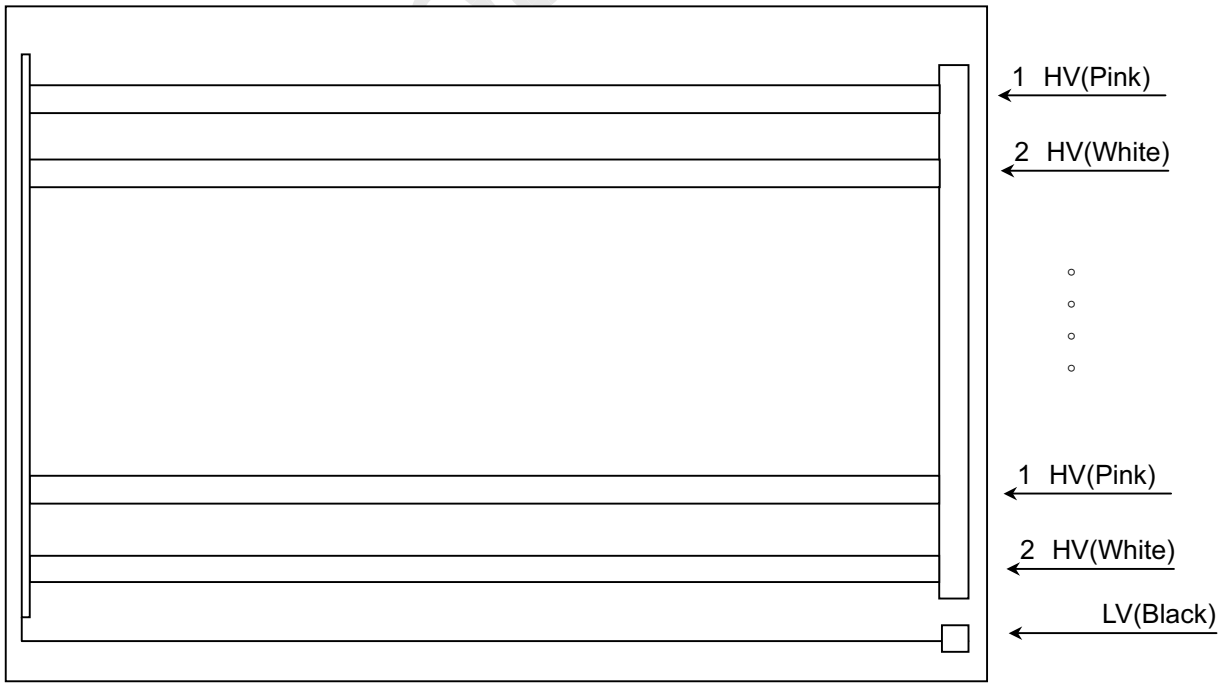
4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



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5. INPUT TERMINAL PIN ASSIGNMENT

5.1 J1 (Master) : Left side (Front View)

Signal Description (J1)

Pin	Name	Description
1	NC	Not connection Should keep open.
2	NC	Not connection Should keep open.
3	NC	Not connection Should keep open.
4	NC	Not connection Should keep open.
5	NC	Not connection Should keep open.
6	DGND	Digital Ground
7	SDA	I2C data for gamma adjustment/brightness (3.3V typ)
8	SCL	I2C clock for gamma adjustment/brightness (3.3V typ)
9	DGND	Digital Ground
10	LGND	LVDS Ground
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXO3-	Negative LVDS differential data input. Channel O3 (odd)
13	RXOC+	Positive LVDS differential clock input. (odd)
14	RXOC-	Negative LVDS differential clock input. (odd)
15	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
16	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
17	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
18	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
19	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
20	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
21	RXE3+	Positive LVDS differential data input. Channel E3 (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXEC+	Positive LVDS differential clock input. (even)
24	RXEC-	Negative LVDS differential clock input. (even)
25	RXE2+	Positive LVDS differential data input. Channel E2 (even)
26	RXE2-	Negative LVDS differential data input. Channel E2 (even)
27	RXE1+	Positive LVDS differential data input. Channel E1 (even)
28	RXE1-	Negative LVDS differential data input. Channel E1 (even)
29	RXE0+	Positive LVDS differential data input. Channel E0 (even)
30	RXE0-	Negative LVDS differential data input. Channel E0 (even)
31	LGND	LVDS Ground

5.2 J2(Slave) : Right side(Front View)

Signal Description (J2)

Pin	Name	Description
1	BLON	Backlight on/off signal (HI:backlight ON, Low:backlight OFF)
2	VDIM-IN	Brightness Dimming Control Voltage(0~3V, 0V:MaxBrightness)
3	VDIM-OUT	Brightness Dimming Control Voltage Output Generated by I2C command
4	NC	Not connection Should keep open.
5	NC	Not connection Should keep open.
6	DGND	Digital Ground
7	NC	Not connection Should keep open.
8	NC	Not connection Should keep open.
9	DGND	Digital Ground
10	LGND	LVDS Ground
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXO3-	Negative LVDS differential data input. Channel O3 (odd)

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13	RXOC+	Positive LVDS differential clock input. (odd)
14	RXOC-	Negative LVDS differential clock input. (odd)
15	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
16	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
17	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
18	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
19	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
20	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
21	RXE3+	Positive LVDS differential data input. Channel E3 (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXEC+	Positive LVDS differential clock input. (even)
24	RXEC-	Negative LVDS differential clock input. (even)
25	RXE2+	Positive LVDS differential data input. Channel E2 (even)
26	RXE2-	Negative LVDS differential data input. Channel E2 (even)
27	RXE1+	Positive LVDS differential data input. Channel E1 (even)
28	RXE1-	Negative LVDS differential data input. Channel E1 (even)
29	RXE0+	Positive LVDS differential data input. Channel E0 (even)
30	RXE0-	Negative LVDS differential data input. Channel E0 (even)
31	LGND	LVDS Ground

Note (1) Connector Part No.: JAE-FI-WE31P-HFE or equivalent.

Note (2) The first pixel is even.

Note (3) Input signal of even and odd clock should be the same timing.

Note (4) You can adjust brightness by two methods, one is by I2C function of J1, the other is by pin 11 of Inverter connector(CN1). If you select one method to adjust brightness, another method's input pin(s) should be floating.

Note (5) If you don't use I2C to program gamma or adjust brightness by J1, you should make the pin7, pin8 of J1 open.

Note (6) The module uses a 100-ohm resistor between positive and negative data lines of each receiver input.

5.3 LVDS Input Data Order

LVDS interface receiver required input data mapping table								
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG2	ER7	ER6	ER5	ER4	ER3	ER2
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB3	EB2	EG7	EG6	EG5	EG4	EG3
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB7	EB6	EB5	EB4
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB1	EB0	EG1	EG0	ER1	ER0
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG2	OR7	OR6	OR5	OR4	OR3	OR2
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB3	OB2	OG7	OG6	OG5	OG4	OG3
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB7	OB6	OB5	OB4
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB1	OB0	OG1	OG0	OR1	OR0

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5.4 DC/DC Connector Signal (J601)

Pin No.	Symbol	Description
1-4	Gnd	Ground for Vcc line
5-8	Vcc	+12.0V Power Supply for Control board

Note (1) Connector Part No.: IL-Z-8PL-SMTYE or equivalent

Note (2) User's connector Part No.: IL-Z-8S-S125C3 (JAE)

5.5 Inverter Input Signal(CN1)

Pin No.	Symbol	Description
1	Vin	Input voltage
2	Vin	Input voltage
3	Vin	Input voltage
4	Vin	Input voltage
5	Vin	Input voltage
6	Gnd	Ground
7	Gnd	Ground
8	Gnd	Ground
9	Gnd	Ground
10	Gnd	Ground
11	VDIM	Brightness control (0~3V)
12	BLON	Inverter On/Off control (0/3.3V)

Note (1) Connector Part No.: S12B-PH-SM3-TB (JST) or equivalent

Note (2) User's connector Part No.: PHR-12 (JST)

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	G5	G4	G3	G2	G1	G0	R7	R6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

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Scale Of Green	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATION

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	Fc	60	65	66	MHz	-
	Period	Tc	15.15	15.38	16.66	ns	
	High Time	Tch	-	4/7	-	Tc	-
	Low Time	Tcl	-	3/7	-	Tc	-
LVDS Data	Setup Time	Tlvs	600	-	-	ps	-
	Hold Time	Tlvh	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	Fr	-	60	-	Hz	Tv=Tvd+Tvb
	Total	Tv	1546	1612	1628	Th	-
	Display	Tvd	1536	1536	1536	Th	-
	Blank	Tvb	Tv-Tvd	76	Tv-Tvd	Th	-
Horizontal Active Display Term	Total	Th	640	672	700	Tc	Th=Thd+Thb
	Display	Thd	512	512	512	Tc	-
	Blank	Thb	Th-Thd	160	Th-Thd	Tc	-

Note: Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM

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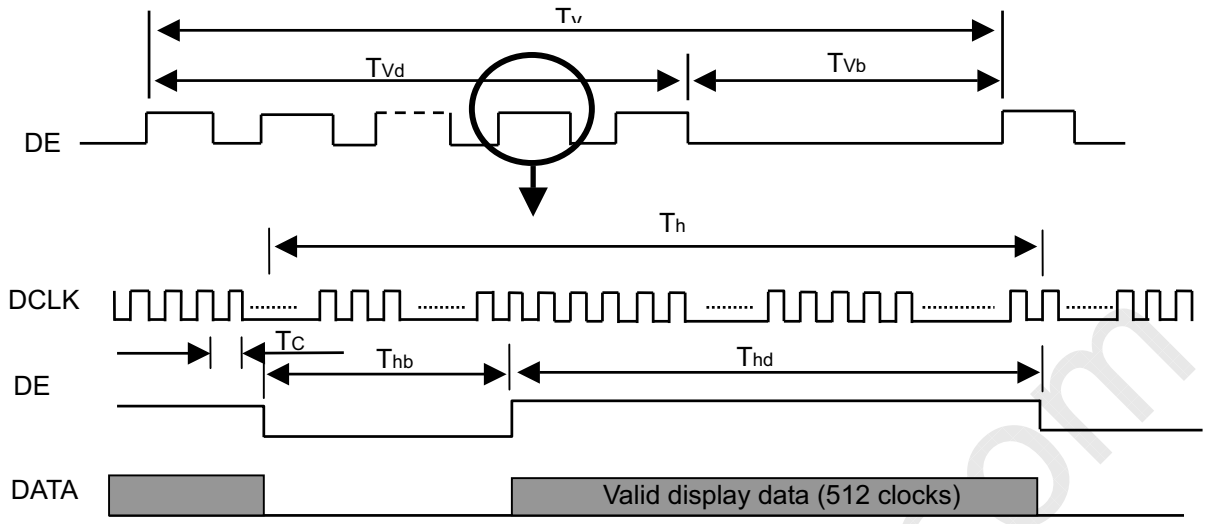

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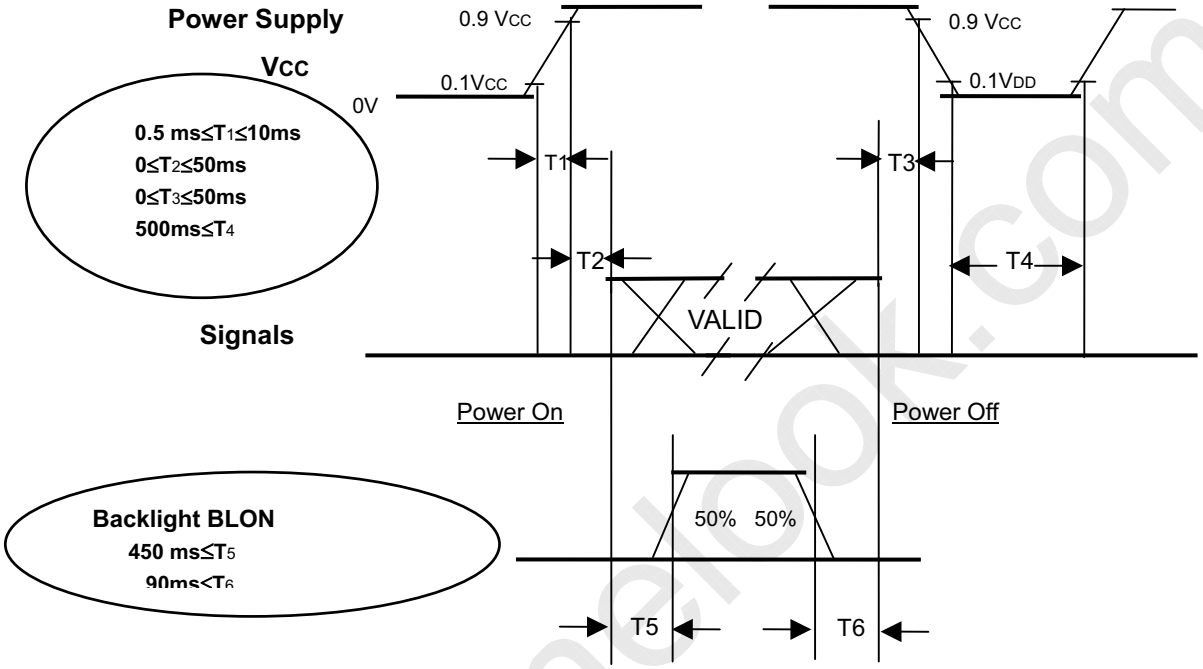
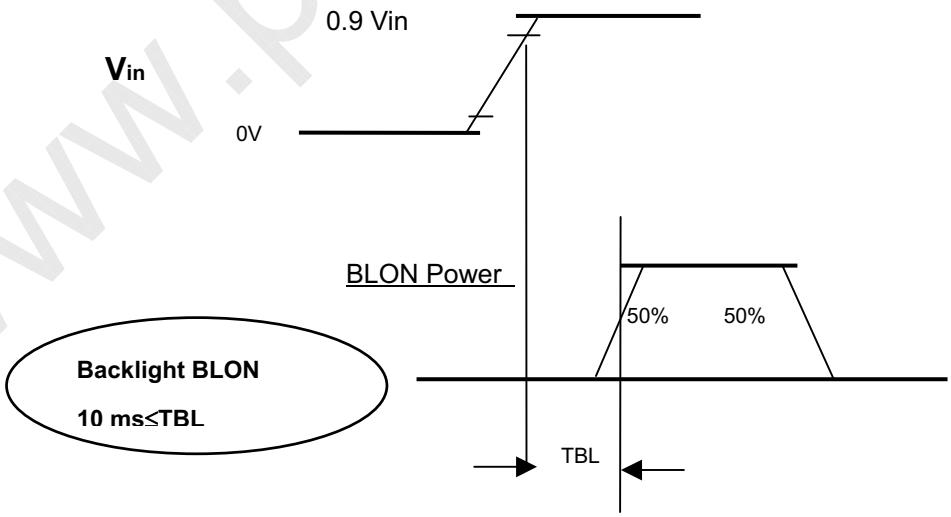
6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the inverter power on and signal power on/off sequence should be as the diagram below.



Power ON/OFF Sequence



Inverter Power ON Sequence

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Note.

(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 OPTICAL SPECIFICATION

The relative measurement methods of optical characteristics are shown in 7.1. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rx	θ_x=0°, θ_Y =0° CS-1000	Typ – 0.03	0.649	Typ + 0.03		(1), (5)
		Ry			0.323			
	Green	Gx			0.291			
		Gy			0.618			
	Blue	Bx			0.142			
		By			0.086			
	White	Wx			0.294			
		Wy			0.309			
Center Luminance of White		L_C		500	600	-	cd/m^2	(4), (5)
Contrast Ratio		CR		500	600	-	-	(2), (5)
Response Time		T_R	θ_x=0°, θ_Y =0°	-	25		ms	(3)
		T_F		-	25		ms	
White Variation		δW	θ_x=0°, θ_Y =0° USB2000	-	1.25	1.40	-	(5), (6)
Viewing Angle	Horizontal	θ_x+	CR ≧ 10 USB2000	80	85	-	Deg.	(1), (5)
		θ_x-		80	85	-		
	Vertical	θ_Y+		80	85	-		
		θ_Y-		80	85	-		

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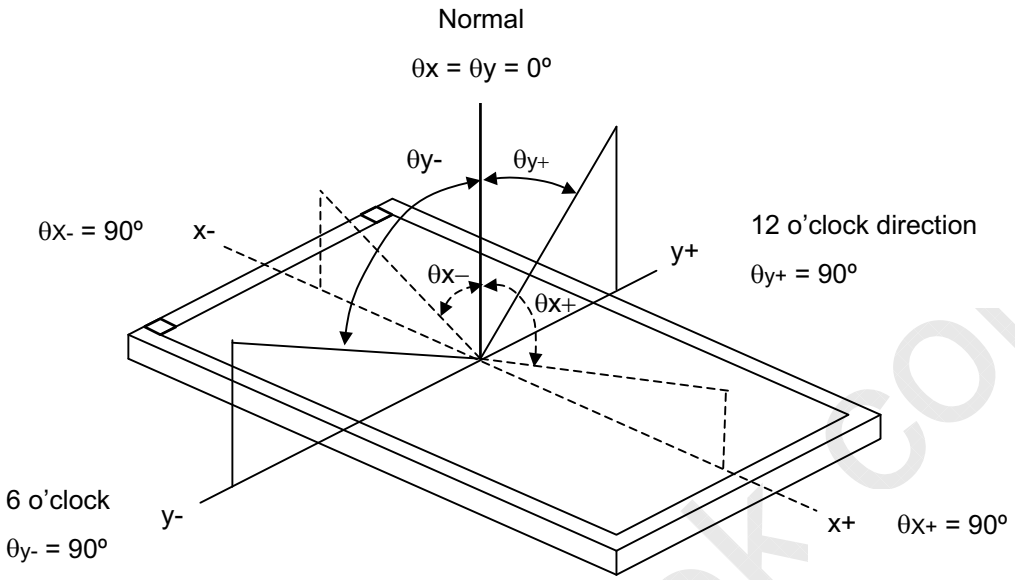
Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

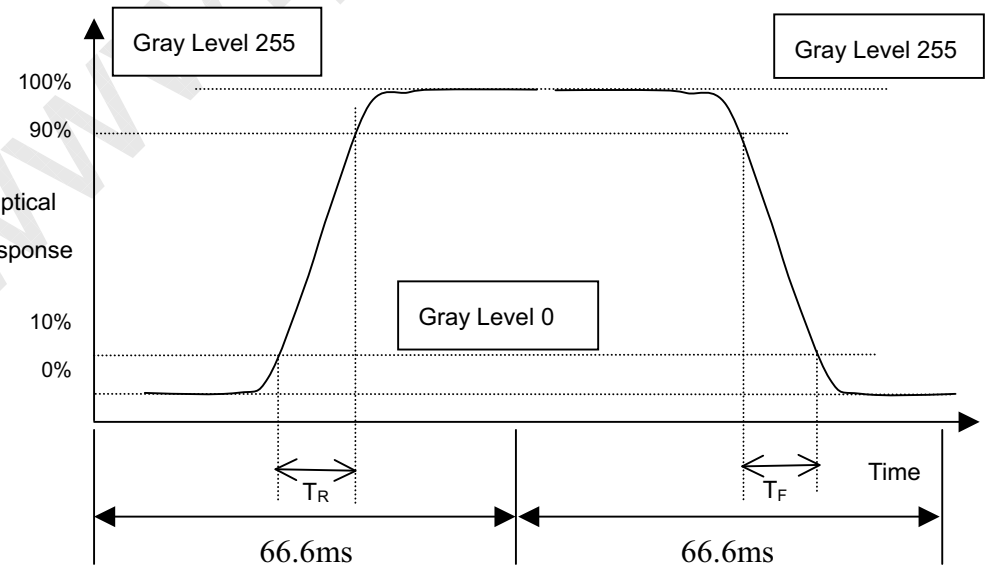
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (7).

Note (3) Definition of Response Time (T_R, T_F):



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Note (4) Definition of Luminance of White (L_C):

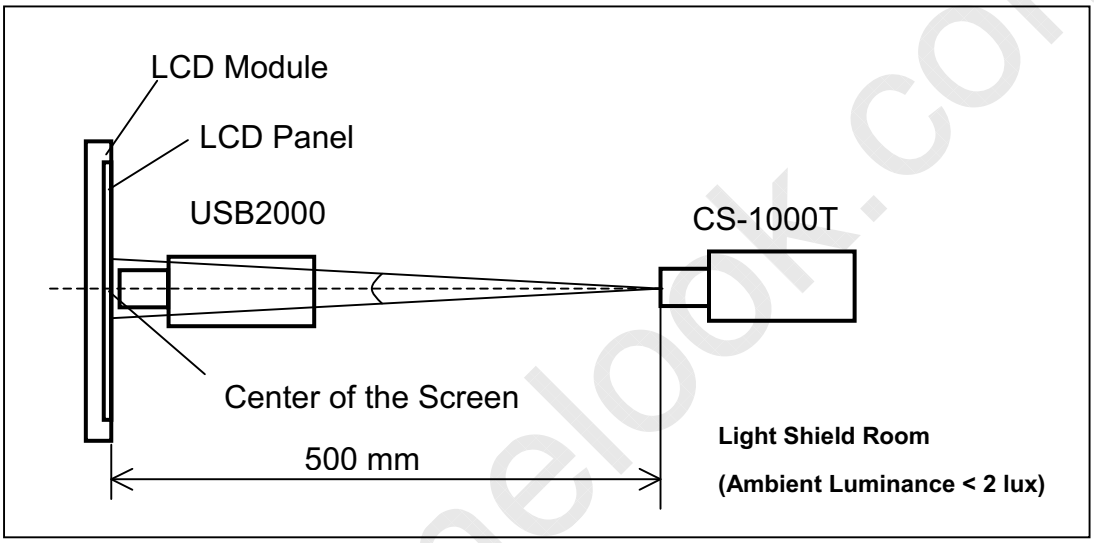
Measure the luminance of gray level 255 at center point

L_C = L (5)

L (x) is corresponding to the luminance of the point X at Figure in Note (7).

Note (5) Measurement Setup:

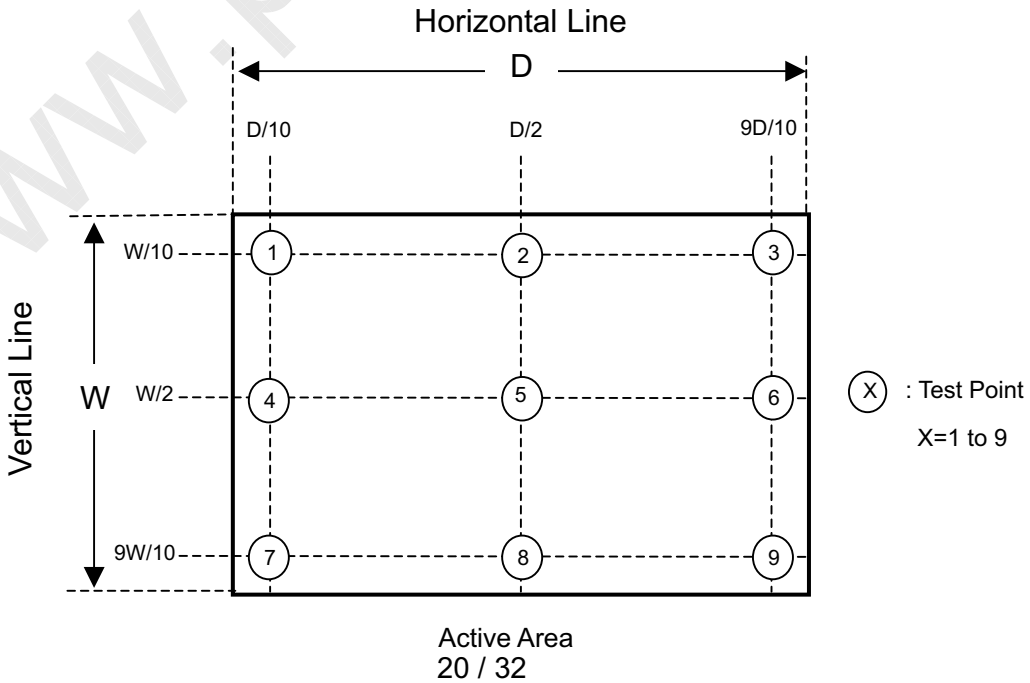
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2) ……L (4), L (9)] / Minimum [L (1), L (2) …… L (4), L (9)]



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7.2 Image Retention

The panel spec of image sticking / retention is as follows.

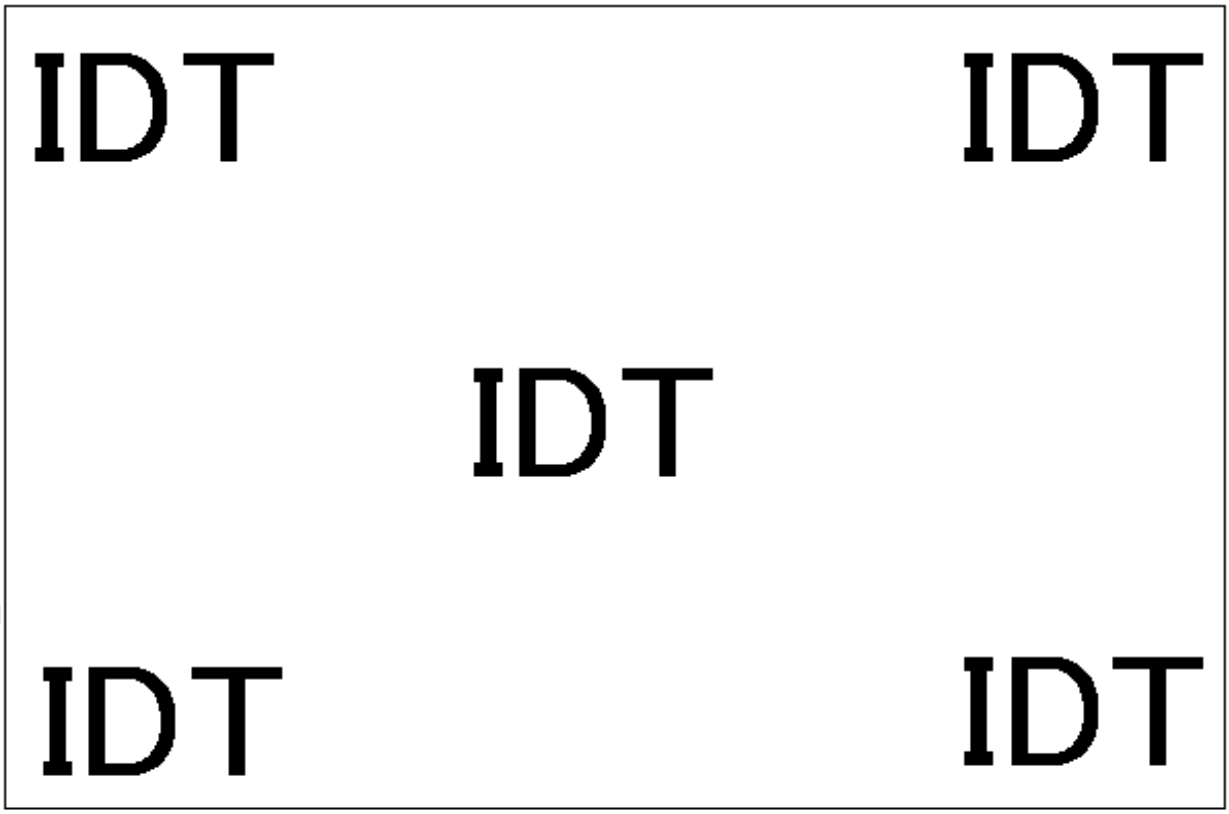
Test method: The L0/L255 IDT Logo pattern below is displayed for the display time
Then, change the pattern to L128 All gray pattern and count the time

Spec for Image retention time is below,

Display Time	5sec	60sec	5min
Time until disappearing	**10sec**	**20sec**	**30sec**

Definition of disappearing time: The time when the brightness of IDT logo will reach to 0.89% difference from background level (L128).

$$\frac{|\,L\,logo - L128\,|}{L128} \times 100 \leqq 0.89\%$$



Character : L0
Background : L255

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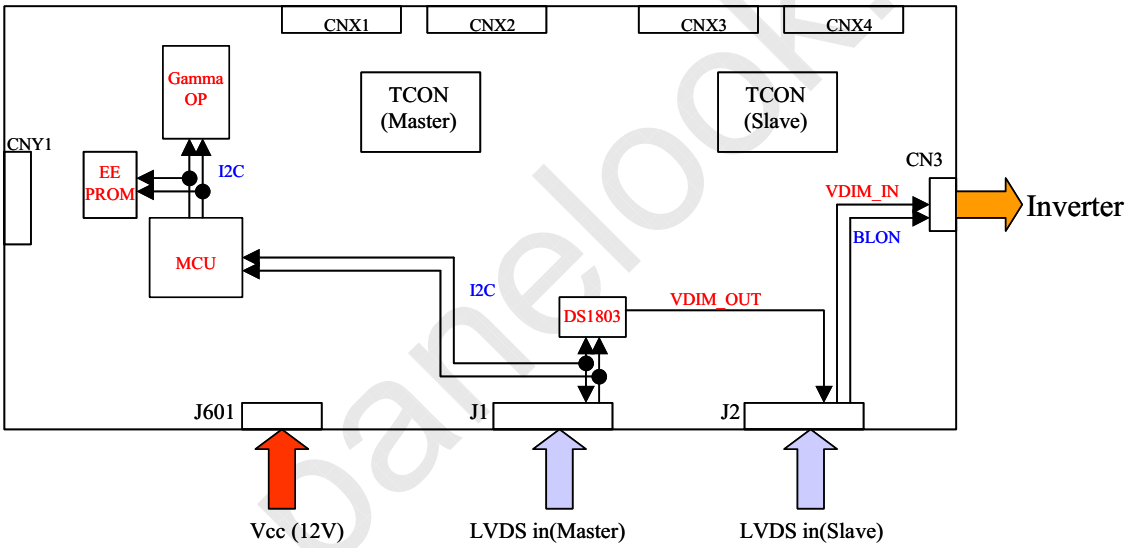
8. Input Parameters Details

8.1 Backlight on/off (BLON) and brightness adjustment (VDIM_IN / VDIM_OUT)

The backlight unit can be controlled to turn on or turn off by BLON signal that is in the pin 1 of J2. The input voltage specification of BLON signal is described in section 3.3. If the input voltage level is low, the backlight unit will be turned off. If high, it will be turned on.

The backlight unit also can be controlled to adjust brightness by VDIM_IN signal that is in pin 2 of J2. The input voltage range is from 0V to 3V. The maximum brightness is acquirement when the input voltage is 0V. If the input voltage is 3V, the backlight unit will present the minimum brightness.

You can use I2C interface protocol to program DS1803 (DAC, Digital-to-Analog Converter) by pin7, 8 of J1. The port-1 of DS1803 will generate one voltage that you want. Then, the voltage is sent to VDIM_OUT signal that is in pin 3 of J2. The systems can feedback this signal to VDIM_IN signal to control the BLU brightness. Please refer to I2C interface protocol in MAXIM DS1803 datasheet for brightness adjustment.



Panel control board interface

8.2 Function of MCU (Micro-Controller Unit) for control panel gamma voltage

Following describes the function of select gamma table. The structure is listed as below. From the main bus, SDA_ISP and SCL_ISP, the MCU can be controlled via the standard I2C interface protocol. Then MCU would send the commands to EEPROM or gamma voltage generator. Then the select operation could be operated. The detailed functions will be described as below.

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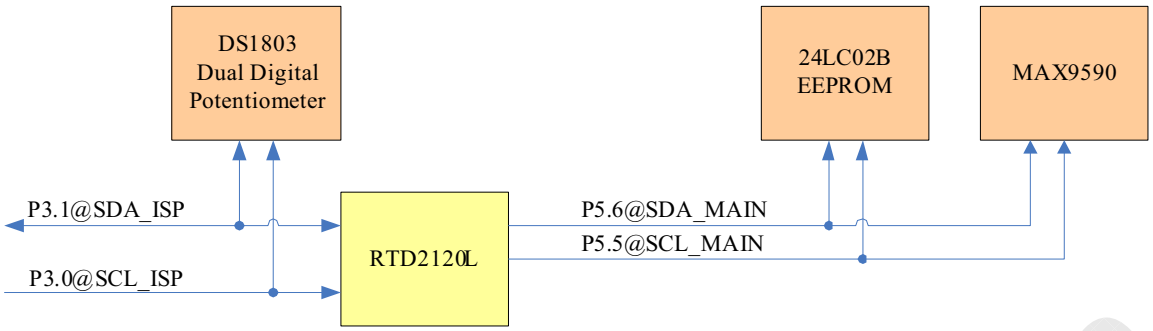
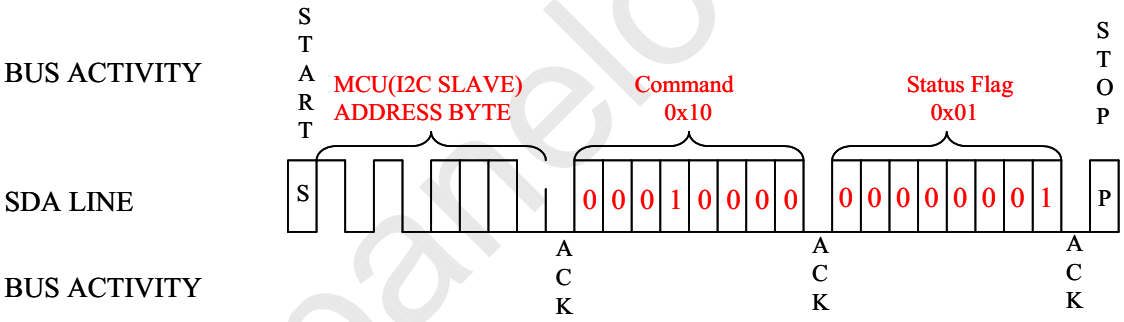
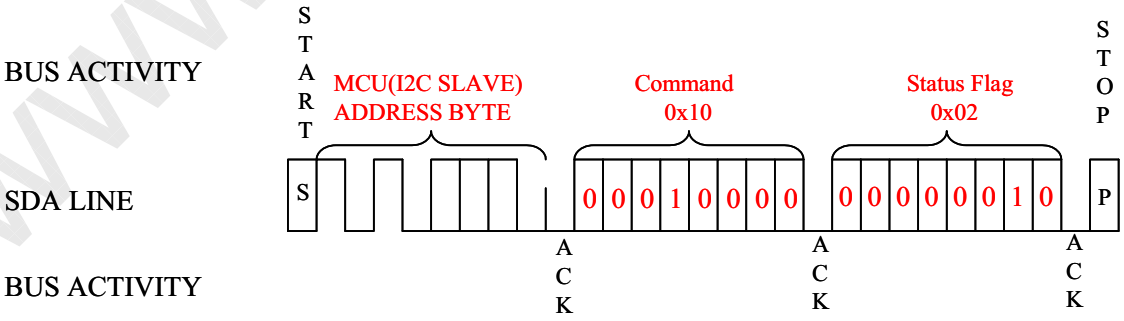


I2C structure of circuit

SELECT OPERATION: A select operation requires 8-bit command word that is following the device address word. After the command word, the MCU should receive information of gamma table. Finally it should terminate the select operation with a stop condition. After select command, there is a status flag for the selection of gamma table. There are two gamma tables for user choice. One is default table (G2.2 curve); another one is user's own DICOM curve. Finally it should terminate the select operation with a stop condition.



The select command of default gamma table (G2.2)



The select command of user gamma table (DICOM)

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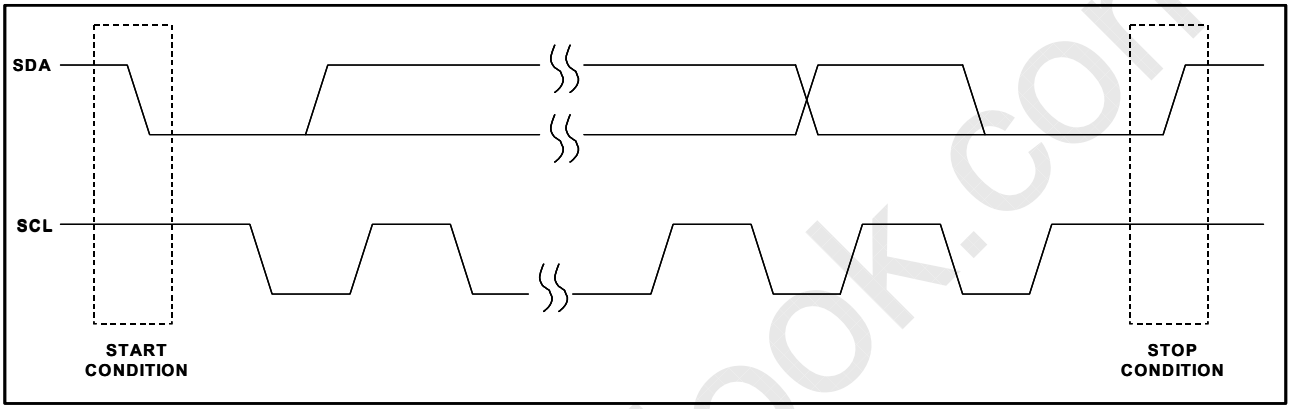
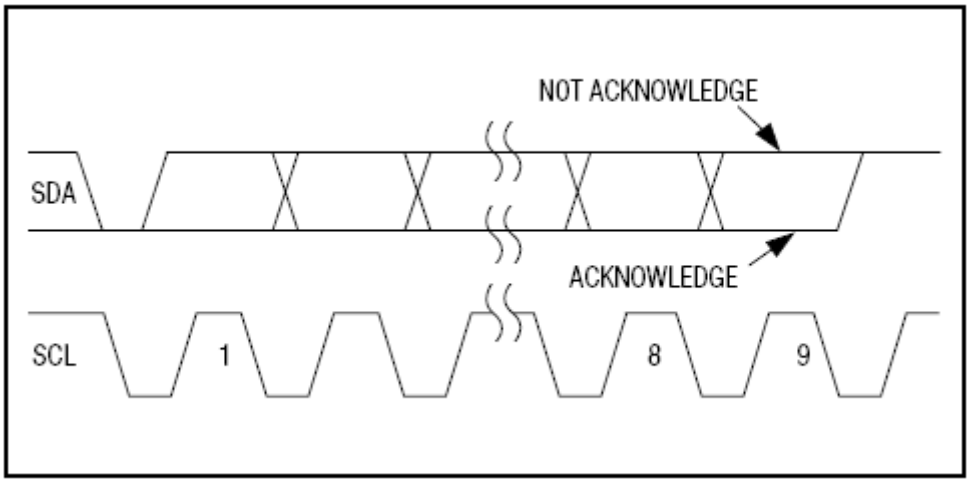
START and STOP Conditions: A master device initiates communication by issuing a START condition (S) which is a high-to-low transition on SDA with SCL high. A START condition from the master signals the beginning of a transmission. The master terminates transmission by a STOP condition (P). A STOP condition is a low-to-high transition on SDA while SCL is high (see the following figure). The STOP condition frees the bus. If a repeated START (Sr) condition is generated instead of a STOP condition, the bus remains active. When a STOP condition or incorrect slave ID is detected, the slave device internally disconnects SCL from the serial interface until the next START or REPEATED START condition, minimizing digital noise and feedthrough.



START/STOP Conditions

Acknowledge Bit (ACK) and Not-Acknowledge Bit (NACK): Successful data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACD). Both the master and the slave generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse(see the following figure).



Acknowledge and Not Acknowledge Bits

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8.3. I2C Specification

Following descriptions show the I2C specifications of the control MCU equipped in the LCD module, which has a gamma adjustment feature. As for the I2C specification of DAC for brightness, please refer to its own specifications (DAC: DALLAS DS1803). 2 signals (SCL and SDA) in the LCD module interface are commonly used for the control of both the gamma adjustment and the DAC.

The address for gamma adjustment is from '1010011'b.

The address for DAC is '0101101'b. Its port-1 is for brightness.

8.3.1 I2C Feature Summary

- Standard mode (100KHz max) support
- 3.3V interface
- Slave mode operation only
- Writing and select gamma table for gamma adjustment

8.3.2 Electrical Specification

2 signals (SCL and SDA) are equipped at the LCD module interface. SCL is the clock input and SDA is the data input/output. These signals should be driven by Open-Drain or Open-Collector without any pull-up resister. Both signals are pulled up by 4.7K ohm resisters to 3.3V(typ.) respectively in the LCD module.

Electrical Specification of I2C Slave

	Symbol	Min	Max	Unit
Input Low voltage	Vil	-0.5	0.5	V
Input High voltage	Vih	2.3	3.6	V
Input Hysteresis voltage	Vhys	0.4	-	V
Input leakage current @ Vil-Min or Vih-Max (*1)	Ii	-30	30	uA
Output Low voltage	Vol	-	0.5	V
Output High impedance leakage current (*3)	Ioh	-30	30	uA

NOTE:

*1: Without pull up resisters (4.7K ohm)

8.3.3 Timing Specification

In the following figure and table, slave is the MCU in the LCD module and master is the scalar to drive the LCD module.

"S" is the START condition and "P" is the STOP condition.

I2C Bus timing

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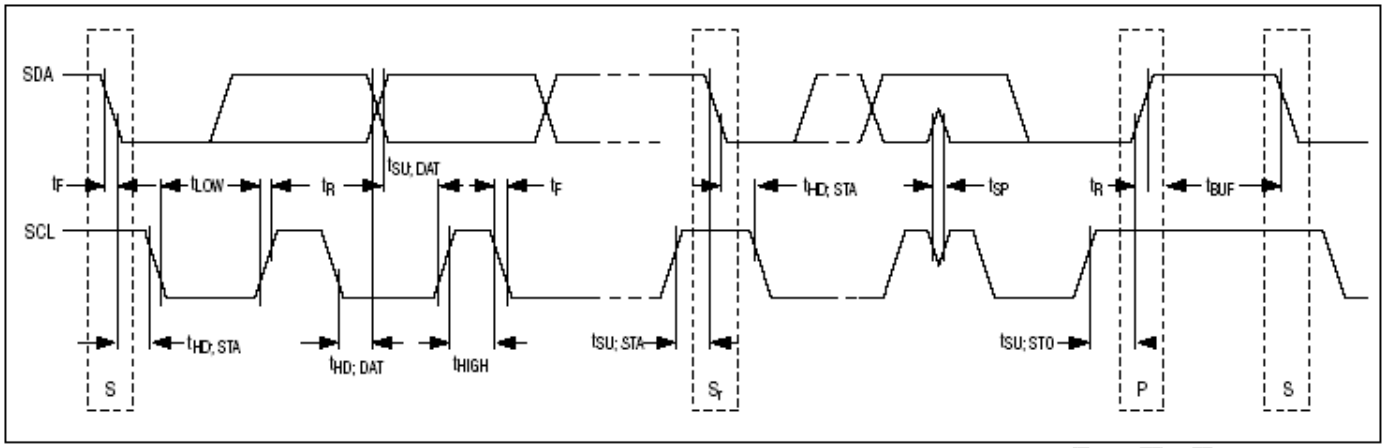

I2C Timing Specification of I2C Slave

	Symbol	Min	Max	Unit	Notes
Frequency of SCL	fSCL	0	100	KHz	
Bus Free Time from STOP to START	tBUF	4.7	-	us	
Setup time of START(Repeated START)	tSU:STA	4.7	-	us	
Hold time of START(Repeated START)	tHD:STA	4.0	-	us	
Low time of SCL	tLOW	4.7	-	us	
High time of SCL	tHIGH	4.0	-	us	
Data hold time	tHD:DAT	0	-	us	
Data setup time	tSU:DAT	250	-	ns	
Rise time	tR	-	1000	ns	
Fall time	tF	-	300	ns	
Setup time of STOP	tSU:STO	4.0	-	us	
Spike suppression	tSP	-	50	ns	

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9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 5 LCD modules / 1 Box

(2) Box dimensions: 468(L) X 402(W) X 591(H) mm

(3) Weight: approximately 15Kg (5 modules per box)

9.2 PACKING METHOD

(1) Carton Packing should have no failure in the following reliability test items.

Test Item	Test Conditions	Note
Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation
Dropping Test	1 Angle, 3 Edge, 6 Face, 60cm	Non Operation

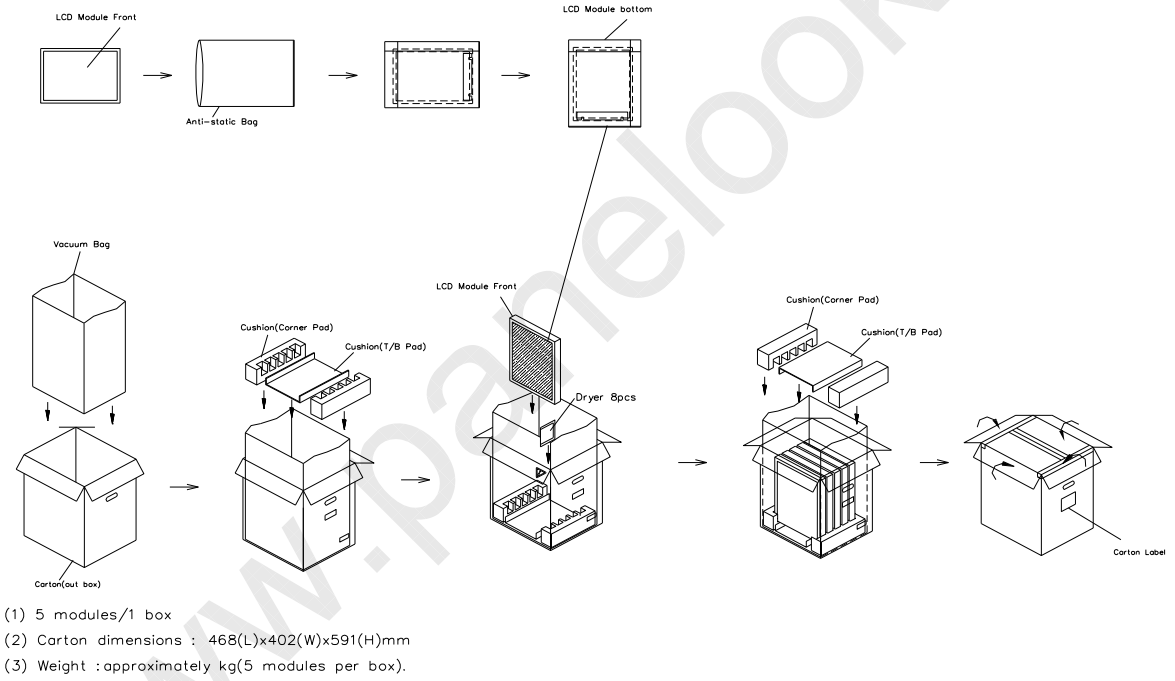

Figure. 9-1 Packing method

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For ocean shipping

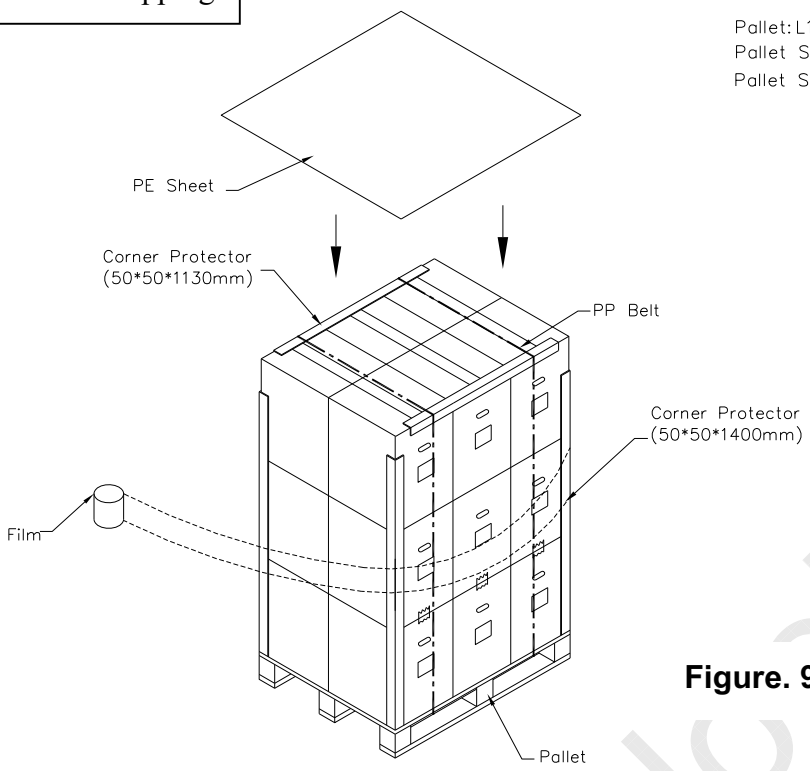

Figure. 9-2 Packing method

For air transport

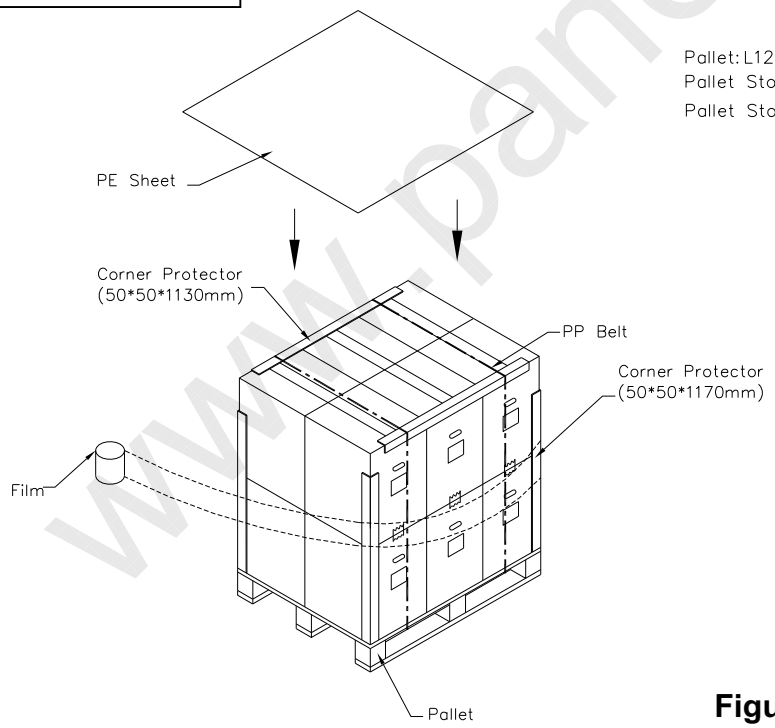

Figure. 9-3 Packing method

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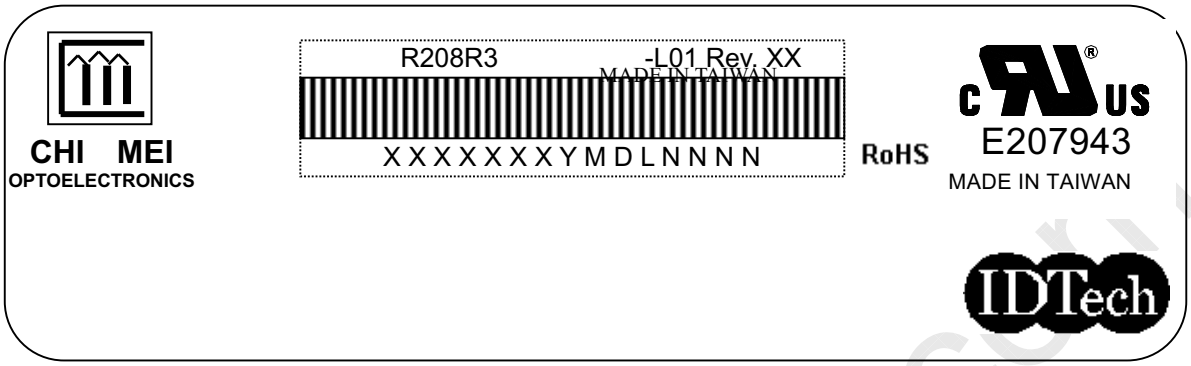
10. DEFINITION OF LABELS

10.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: R208R3-L01

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X X Y M D L N N N N

- Serial No.
- Product Line
- Year, Month, Date
- CMO Internal Use
- CMO Internal Use
- Revision
- CMO Internal Use

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Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4… Month: 1~12=1, 2, 3, ~, 9, A, B, C Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U.
L	Product line #	Line 1=1, Line 2=2, Line 3=3, …
NNNN	Serial number	Manufacturing sequence of product

11. PRECAUTIONS

11.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.

(4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.

(9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(10) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

11.2 SAFETY PRECAUTIONS

(1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

**** End of document ****

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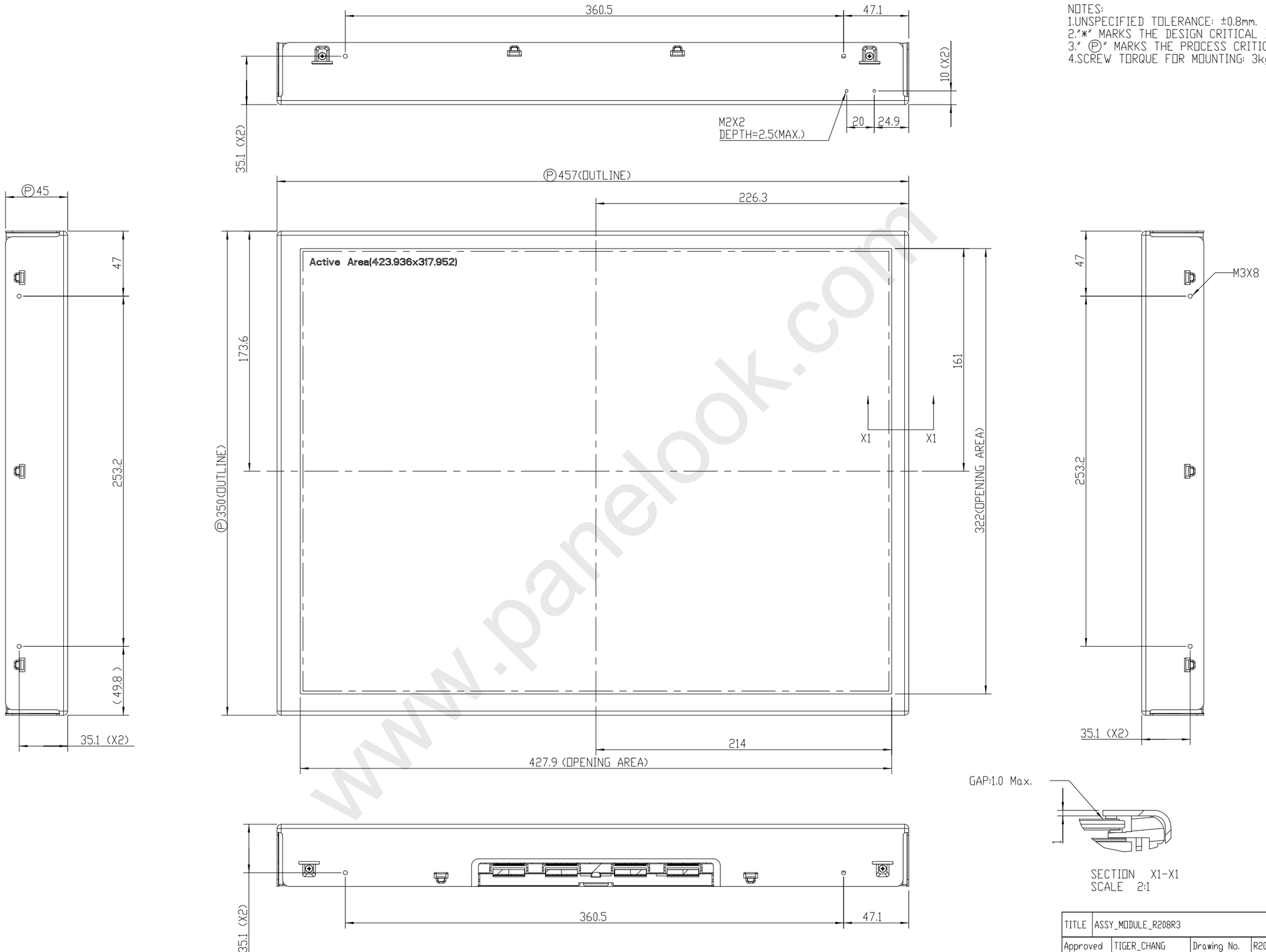
NOTES:
1.UNSPECIFIED TOLERANCE: ±0.8mm.
2."*" MARKS THE DESIGN CRITICAL DIMENSION.
3." Ⓟ " MARKS THE PROCESS CRITICAL DIMENSION.
4.SCREW TORQUE FOR MOUNTING: 3kgf-cm(MAX.)



Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark
B	Add Al Tape	2007.08.29	Honglong	Tiger_Chang	EA0022801	

TITLE	ASSY_MODULE_R208R3					2D REV.	B	
						3D REV.	1.13	
Approved	TIGER_CHANG	Drawing No.	R20814101B					
Checked	ALAN_LEE	Part No.	RK8R301902					
Drawer	HONGLONG_HSU	Material	TBD		Sheet	1 / 2	A2	
Designer	TIGER_CHANG	Date	29-Aug-2007	Scale	1:2	Unit:mm		

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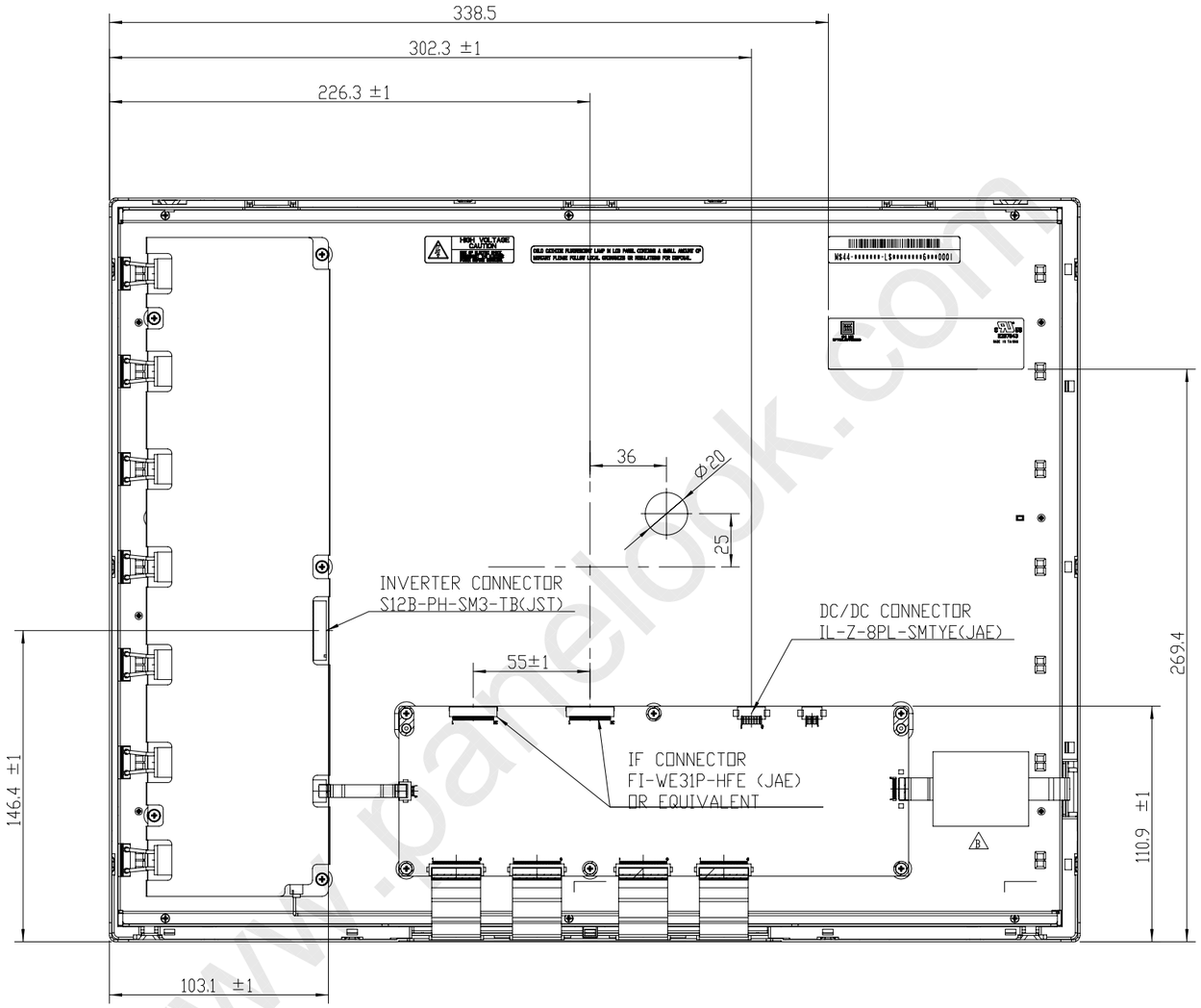

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